HU2103

1A, High Efficiency LDS Module

FEATURES:

- High Density LDS Module
- 1000mA Output Current
- 95% Peak Efficiency at 12VIN
- Input Voltage Range from 4.5V to 17V
- Adjustable Output Voltage
- Enable / PGOOD Function
- Automatic Power Saving/PWM Mode
- Protections (OCP: Non-latching)
- Adjustable Soft Start Function
- Compact Size: 3.5mm*3.5mm*1.7mm
- Pb-free for RoHS compliant
- MSL 2, 260℃ Reflow

APPLICATIONS:

- Point of Load Conversion
- LDOs Replacement
- Set Top Box / DSL Modem / AP Router
- Industrial Personal Computer
-

GENERAL DESCRIPTION:

The LDS module is non-isolated dc-dc converter that can deliver up to 1000mA of output current. The PWM switching regulator, high frequency power inductor are integrated in one hybrid package. It only needs input/output capacitors and one voltage dividing resistor to perform properly.

The module has automatic operation with PWM mode and power saving mode according to loading. Other features include remote enable function, internal soft-start, non-latching over current protection, power good, and input under voltage locked-out capability.

The low profile and compact size package (3.5mm × 3.5mm x 1.7mm) is suitable for automated assembly by standard surface mount equipment. The LDS module is Pb-free and RoHS compliance.

TYPICAL APPLICATION CIRCUIT & PACKAGE:

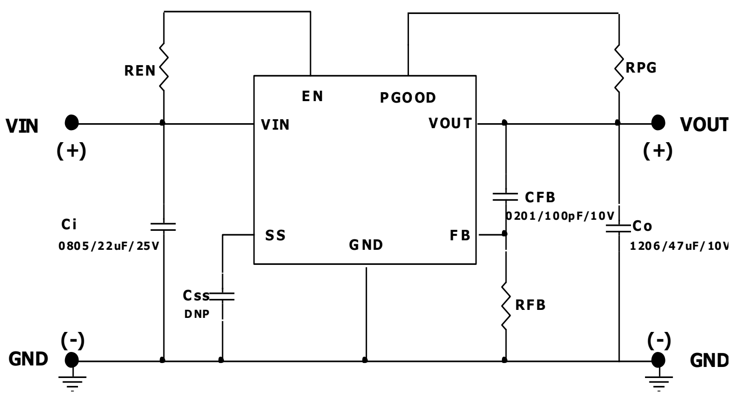

FIG.1 TYPICAL APPLICATION CIRCUIT

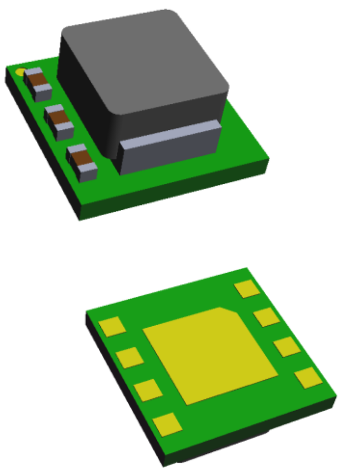

FIG.2 HIGH DENSITY LOW PROFILE LDS MODULE

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1A, High Efficiency LDS Module

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN to GND	Note 1	-	-	+19.0	V
VOUT to GND	Note 1	-	-	+6.5	V
FB to GND	Note 1	-	-	+4.0	V
EN to GND	Note 1	-	-	VIN+0.3	V
PGOOD to GND	Note 1	-	-	+19.0	V
Tc	Case Temperature of Inductor	-	-	+110	°C
Tj	Junction Temperature	-40	-	+125	°C
Tstg	Storage Temperature	-40	-	+125	°C
ESD Rating	Human Body Model (HBM)	-	-	2k	V
	Machine Model (MM)	-	-	200	V
	Charge Device Model (CDM)	-	-	500	V
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+4.5	-	+17.0	V
VOUT	Adjusted Output Voltage	+1.0		+5.0	V
PGOOD	Power Good Voltage	+4.5	-	+17.0	V
Ta	Ambient Temperature	-40	-	+85	°C
■ Thermal Information					
Rth(jchoke-a)	Thermal resistance from junction to ambient. (Note 2)	-	51	-	°C/W

NOTES:
1. Parameters guaranteed and tested by power IC vendor.
2. Rth(jchoke-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 30mm×30mm×1.6mm with 2 layers, 1oz. The test condition is complied with JEDEC EIJ/JESD 51 Standards.

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1A, High Efficiency LDS Module

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, Vin = 12V, Vout = 3.3V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
$I_{Q(IN)}$	Input supply bias current	Vin = 12V, Iout = 0A EN = VIN Vout = 3.3V	-	0.25	-	mA
$I_{S(IN)}$	Input supply current	Vin =12V, EN = VIN	-	-	-	-
		Iout = 1mA Vout = 3.3V	-	0.6	-	mA
		Iout = 100mA Vout = 3.3V	-	33	-	mA
		Iout = 1000mA Vout = 3.3V	-	320	-	mA
■ Output Characteristics						
$I_{OUT(DC)}$	Output continuous current range	Vin=12V, Vout=3.3V	0	-	1000	mA
$V_{O(SET)}$	Ouput voltage set point	With 0.5% tolerance for external resistor used to set output voltage	-3.0		+3.0	% $V_{O(SET)}$
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation accuracy	Vin = 5V to 12V Vout = 3.3V, Iout = 0A Vout = 3.3V, Iout = 1000mA	-	0.1	0.2	% $V_{O(SET)}$
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation accuracy	Iout = 0A to 1000mA Vin = 12V, Vout = 3.3V	-	0.5	1.0	% $V_{O(SET)}$
$V_{OUT(AC)}$	Output ripple voltage	Vin = 12V, Vout = 3.3V EN = VIN	-		-	-
		Iout = 1mA		14		mVp-p
		Iout = 1000mA		8		mVp-p

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1A, High Efficiency LDS Module

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, Vin = 12V, Vout = 3.3V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Control Characteristics						
V_{REF}	Referance voltage	Note 1	0.591	0.600	0.609	V
F_{OSC}	Oscillator frequency	Note 1, PWM Operation		1.0		MHz
V_{UVLO}	Input UVLO threshold	Note1			4.5	V
V_{EN_TH}	Enable rising threshold voltage	Note 1	1.5	-	-	V
	Enable falling threshold voltage	Note 1	-	-	0.4	V
■ Fault Protection						
T_{OTP}	Over temp protection	Note 1	-	150	-	℃
I_{LIMIT_TH}	Current limit threshold	Peak value of inductor current, Note 1	-	2	-	A

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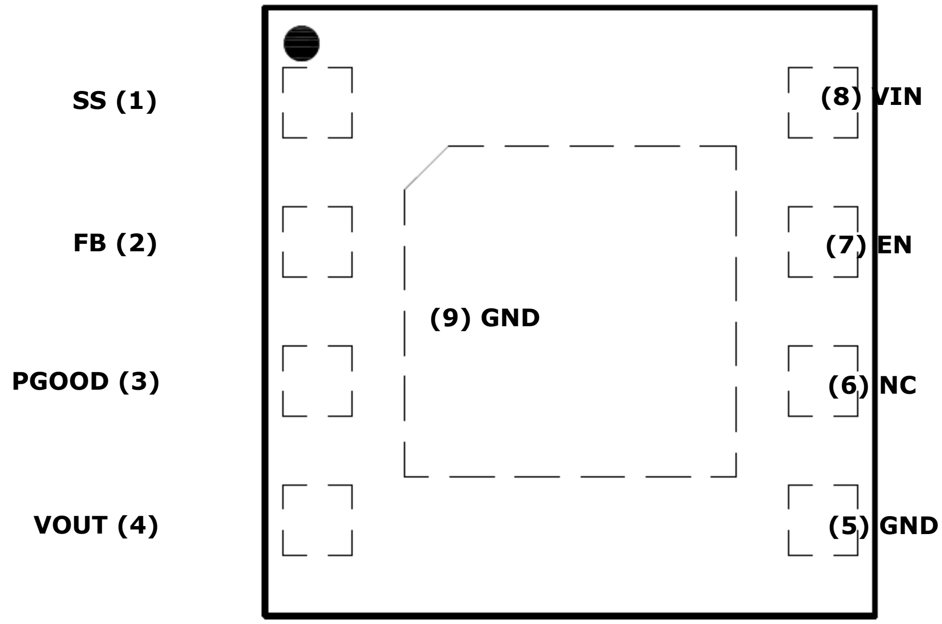
PIN CONFIGURATION:



TOP VIEW

PIN DESCRIPTION:

Symbol	Pin No.	Description
SS	1	Leave SS pin floating for default 1ms soft-start time. For longer than 1ms soft-start time, connect a capacitor from SS to GND. Tss(ms)=Css(nF)*0.6V/4uA
FB	2	Feedback input. Connect an external resistor divider from the output to GND to set the output voltage.
PGOOD	3	Power Good indicator. The pin output is an open drain that can connect to VIN by resistor.
VOUT	4	Power output pin. Connect to output for the load.
GND	5, 9	Power ground pin for signal, input, and output return path. This pin needs to be connected to one or more ground plane directly.
NC	6	No connection
EN	7	On/Off control pin for module. EN = LOW, the module is off. EN = HIGH, the module is on. Do not float.
VIN	8	Power input pin. It needs to be connected to input rail.

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1A, High Efficiency LDS Module

TYPICAL PERFORMANCE CHARACTERISTICS: (1.0VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 42mm×42mm×1.6mm, 4 layers.
The output ripple and transient response are measured by short loop probing and limited to 20MegHz bandwidth.
Cin = 22uF/25V/0805, Cout = 47uF/10V/1206.

The following figures are the typical characteristic curves at 1.0Vout.

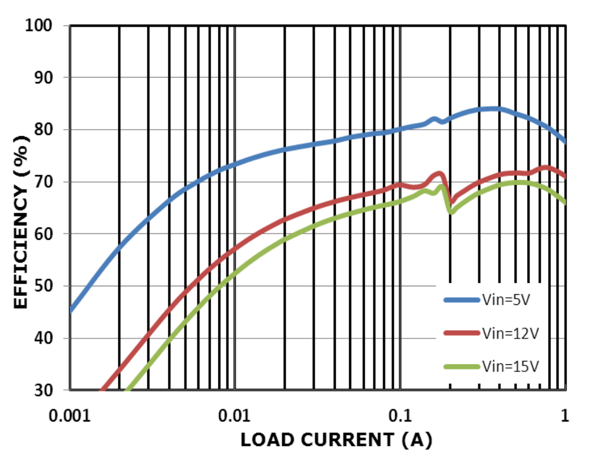

FIG.3 EFFICIENCY V.S. LOAD CURRENT

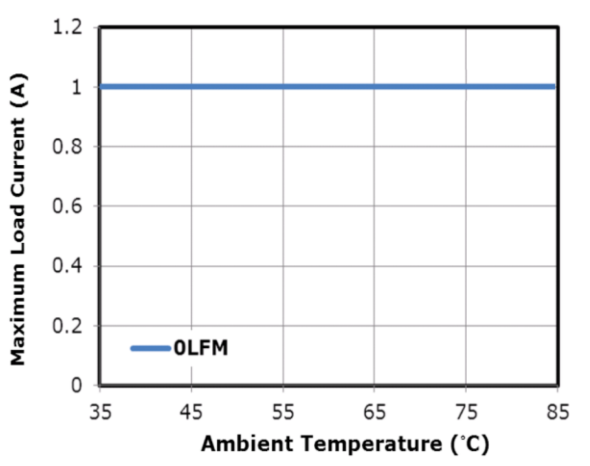

FIG.4 DE-RATING CURVE AT 12VIN

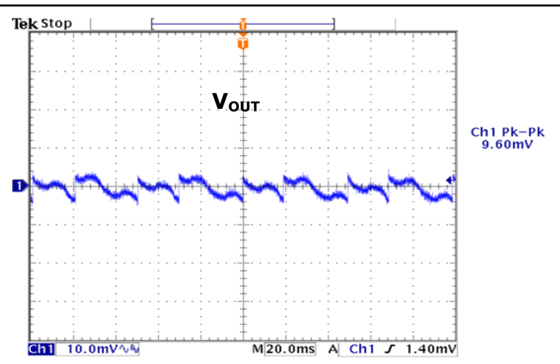

FIG.5 OUTPUT RIPPLE
(12VIN, IOUT=0A)

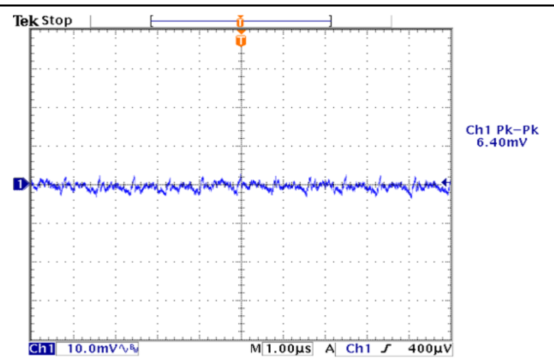

FIG.6 OUTPUT RIPPLE
(12VIN, IOUT=1A)

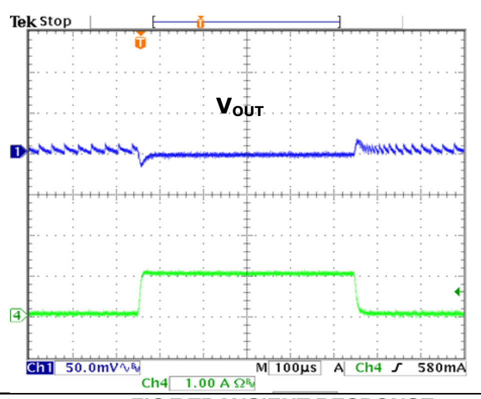

FIG.7 TRANSIENT RESPONSE
(12VIN, 0% to 100% LOAD STEP)

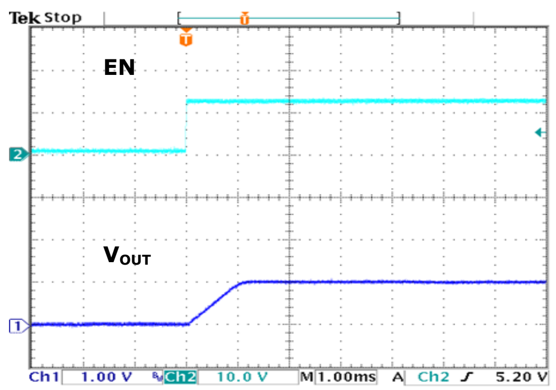

FIG.8 TURN-ON
(12VIN, IOUT=1A)

TYPICAL PERFORMANCE CHARACTERISTICS: (1.2VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 42mm×42mm×1.6mm, 4 layers.
The output ripple and transient response are measured by short loop probing and limited to 20MegHz bandwidth.
Cin = 22uF/25V/0805, Cout = 47uF/10V/1206.

The following figures are the typical characteristic curves at 1.2Vout.

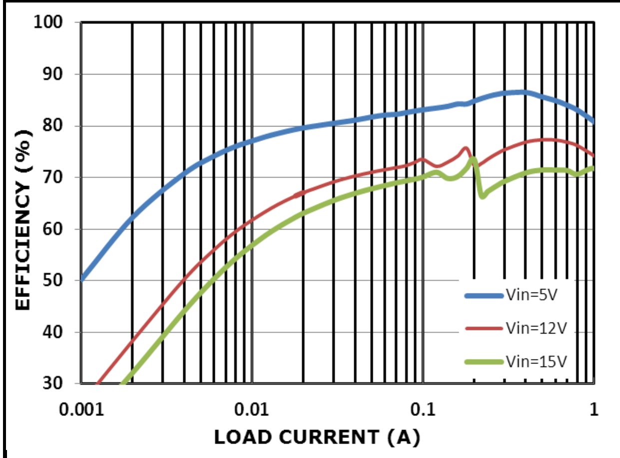

FIG.9 EFFICIENCY V.S. LOAD CURRENT

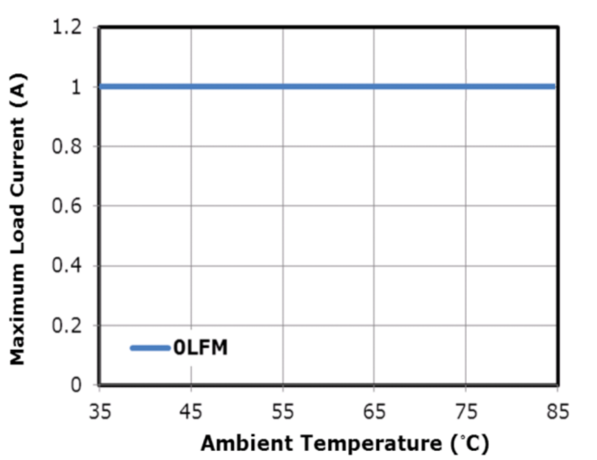

FIG.10 DE-RATING CURVE AT 12VIN

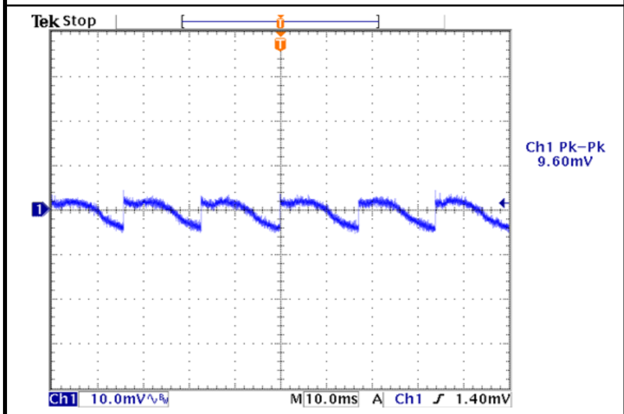

FIG.11 OUTPUT RIPPLE
(12VIN, IOUT=0A)

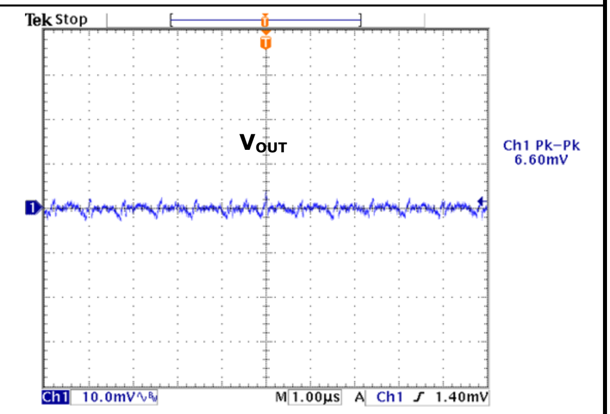

FIG.12 OUTPUT RIPPLE
(12VIN, IOUT=1A)

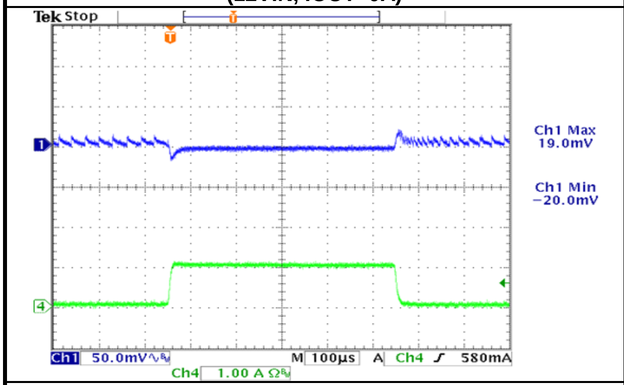

FIG.13 TRANSIENT RESPONSE
(12VIN, 0% to 100% LOAD STEP)

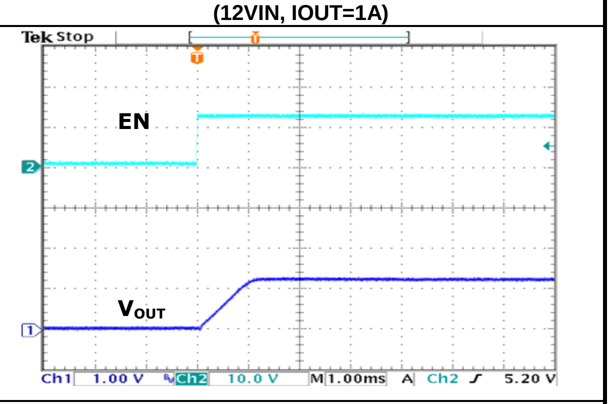

FIG.14 TURN-ON
(12VIN, IOUT=1A)

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1A, High Efficiency LDS Module

TYPICAL PERFORMANCE CHARACTERISTICS: (1.5VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 42mm×42mm×1.6mm, 4 layers.
The output ripple and transient response are measured by short loop probing and limited to 20MegHz bandwidth.
Cin = 22uF/25V/0805, Cout = 47uF/10V/1206.

The following figures are the typical characteristic curves at 1.5Vout.

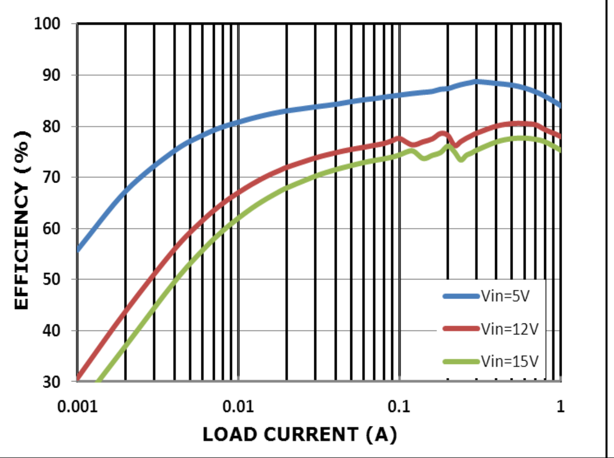

FIG.15 EFFICIENCY V.S. LOAD CURRENT

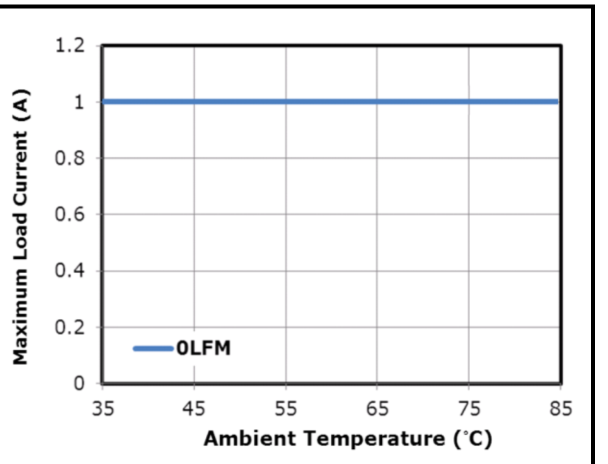

FIG.16 DE-RATING CURVE AT 12VIN

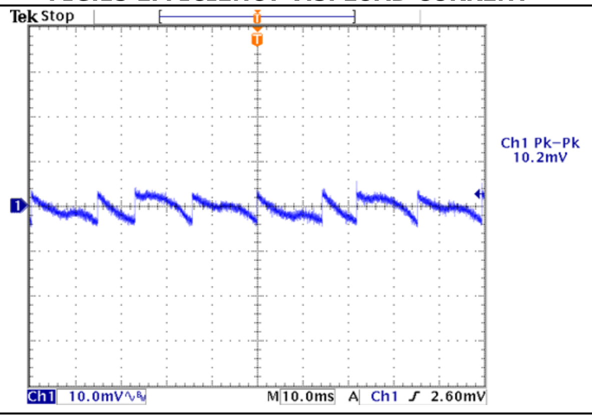

FIG.17 OUTPUT RIPPLE (12VIN, IOUT=0A)

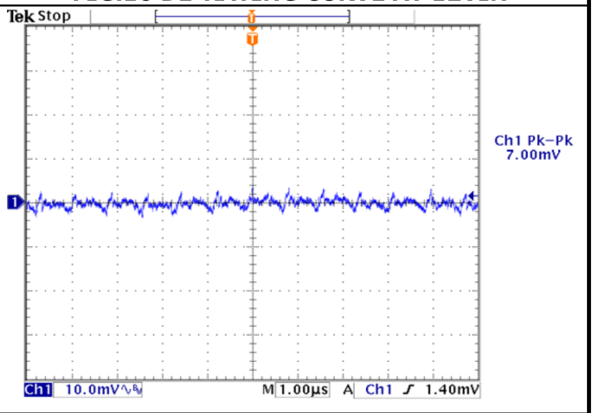

FIG.18 OUTPUT RIPPLE (12VIN, IOUT=1A)

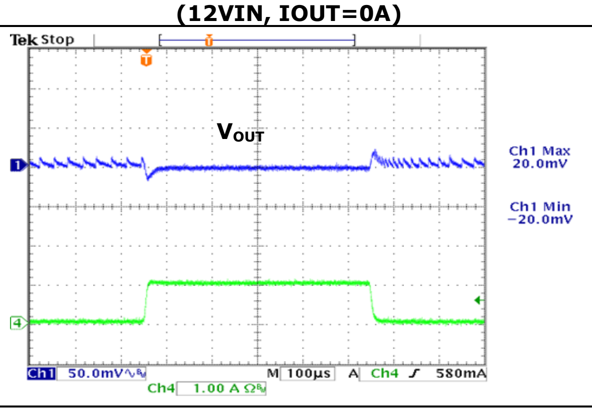

FIG.19 TRANSIENT RESPONSE (12VIN, 0% to 100% LOAD STEP)

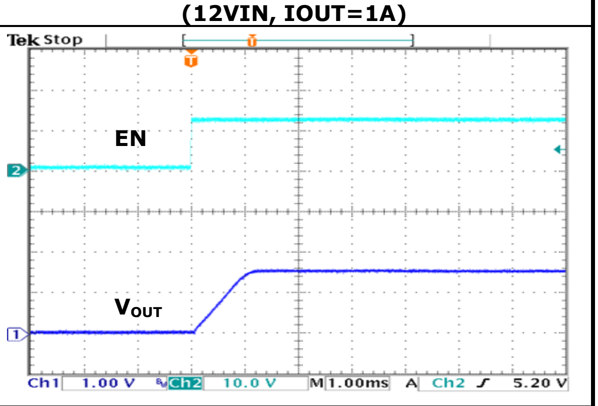

FIG.20 TURN-ON (12VIN, IOUT=1A)

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1A, High Efficiency LDS Module

TYPICAL PERFORMANCE CHARACTERISTICS: (1.8VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 42mm×42mm×1.6mm, 4 layers.
The output ripple and transient response are measured by short loop probing and limited to 20MegHz bandwidth.
Cin = 22uF/25V/0805, Cout = 47uF/10V/1206.

The following figures are the typical characteristic curves at 1.8Vout.

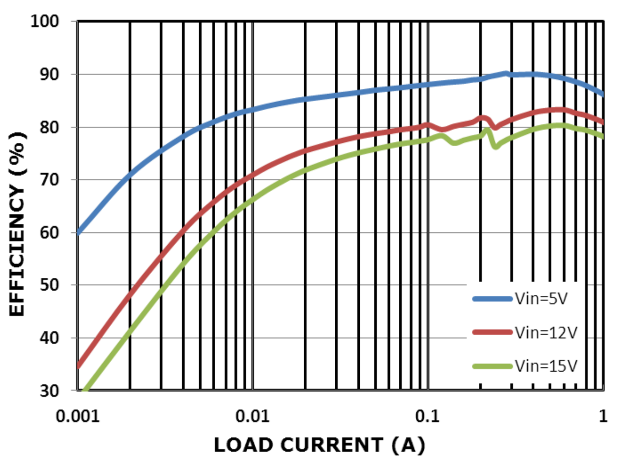

FIG.21 EFFICIENCY V.S. LOAD CURRENT

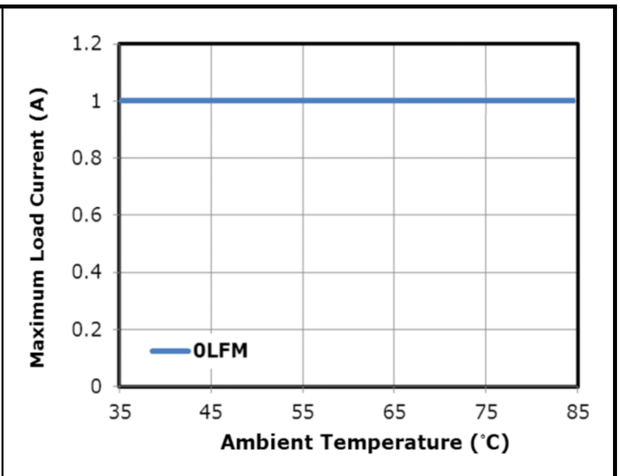

FIG.22 DE-RATING CURVE AT 12VIN

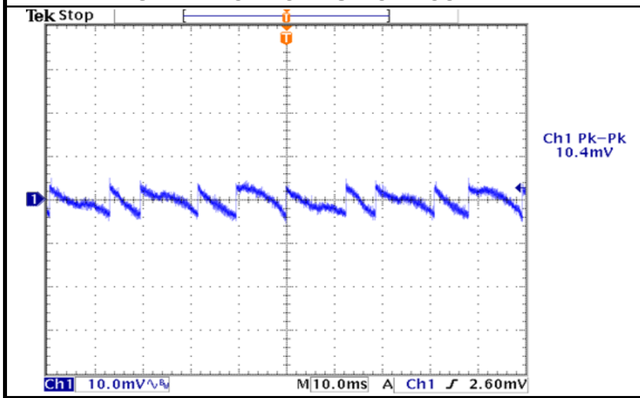

FIG.23 OUTPUT RIPPLE
(12VIN, IOUT=0A)

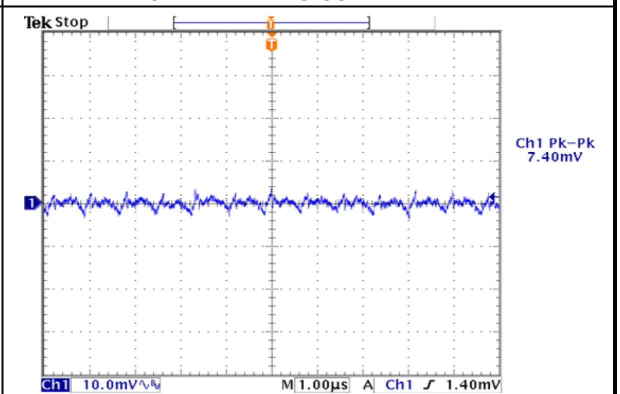

FIG.24 OUTPUT RIPPLE
(12VIN, IOUT=1A)

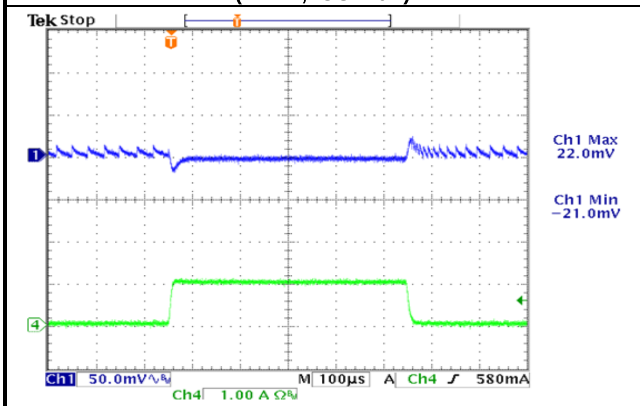

FIG.25 TRANSIENT RESPONSE
(12VIN, 0% to 100% LOAD STEP)

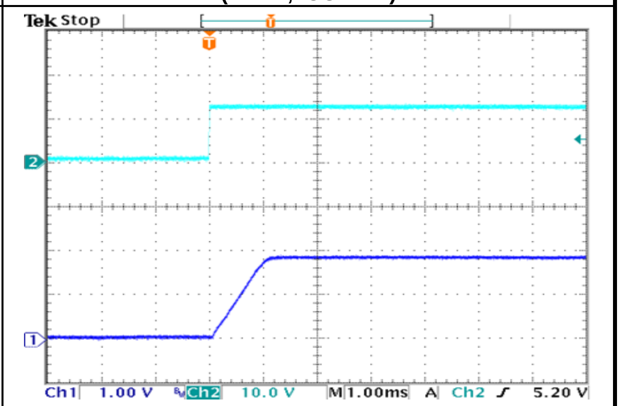

FIG.26 TURN-ON
(12VIN, IOUT=1A)

TYPICAL PERFORMANCE CHARACTERISTICS: (2.5VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 42mm×42mm×1.6mm, 4 layers.
The output ripple and transient response are measured by short loop probing and limited to 20MegHz bandwidth.
Cin = 22uF/25V/0805, Cout = 47uF/10V/1206.

The following figures are the typical characteristic curves at 2.5Vout.

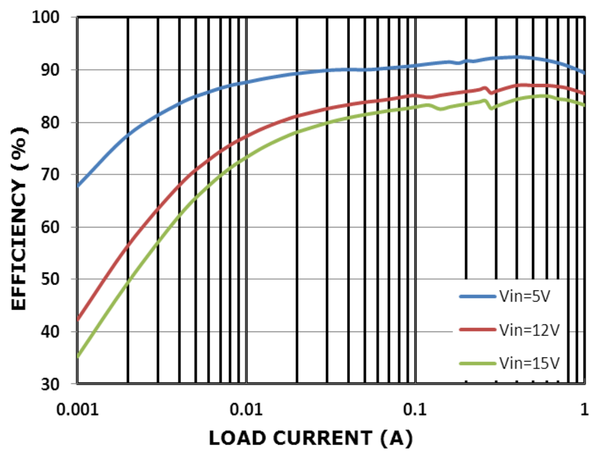

FIG.27 EFFICIENCY V.S. LOAD CURRENT

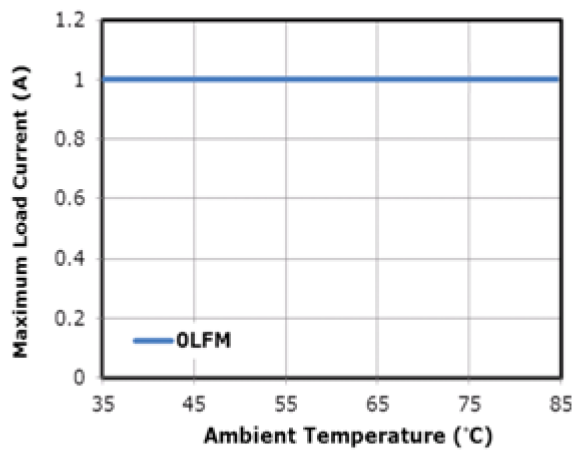

FIG.28 DE-RATING CURVE AT 12VIN

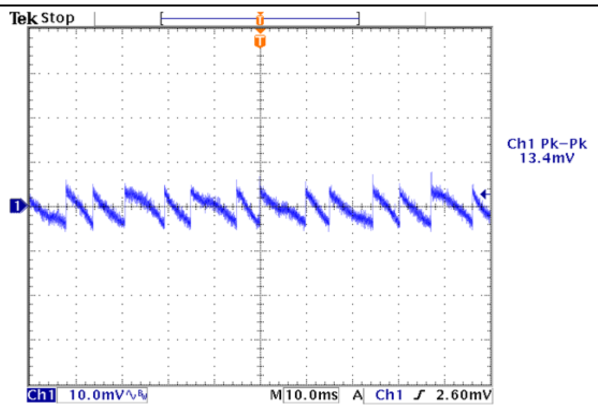

FIG.29 OUTPUT RIPPLE
(12VIN, IOUT=0A)

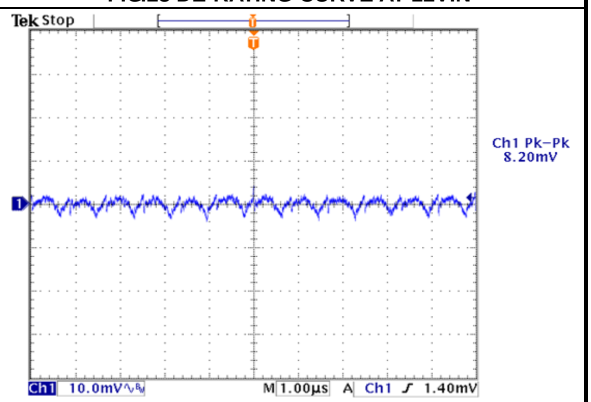

FIG.30 OUTPUT RIPPLE
(12VIN, IOUT=1A)

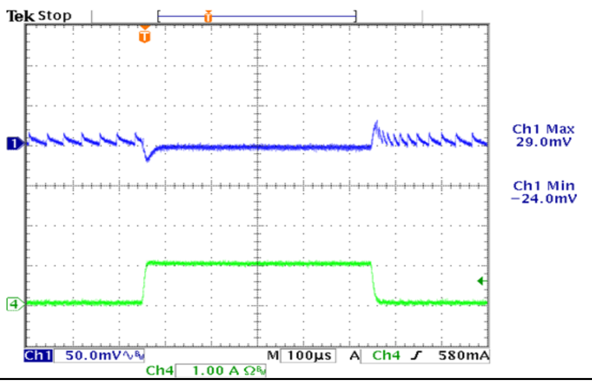

FIG.31 TRANSIENT RESPONSE
(12VIN, 0% to 100% LOAD STEP)

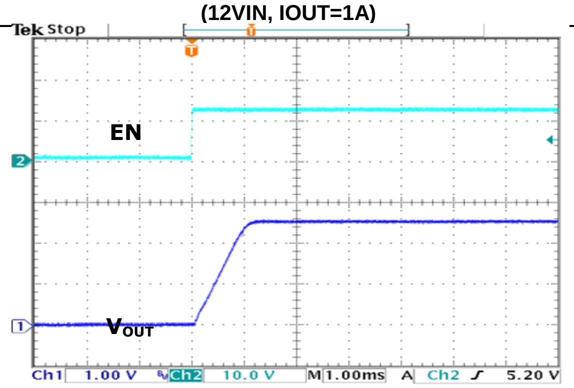

FIG.32 TURN-ON
(12VIN, IOUT=1A)

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1A, High Efficiency LDS Module

TYPICAL PERFORMANCE CHARACTERISTICS: (3.3VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 42mm×42mm×1.6mm, 4 layers.
The output ripple and transient response are measured by short loop probing and limited to 20MegHz bandwidth.
Cin = 22uF/25V/0805, Cout = 47uF/10V/1206.

The following figures are the typical characteristic curves at 3.3Vout.

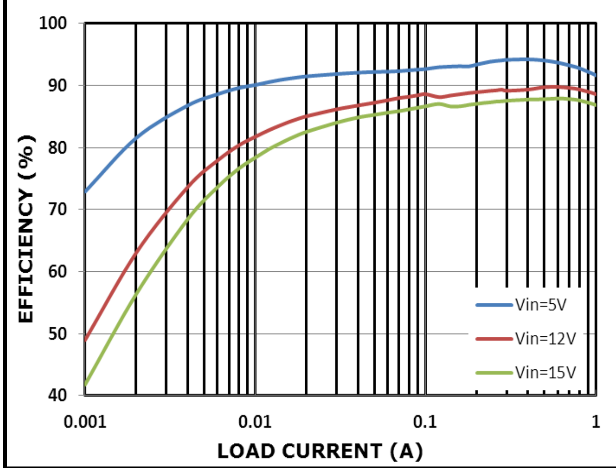

FIG.33 EFFICIENCY V.S. LOAD CURRENT

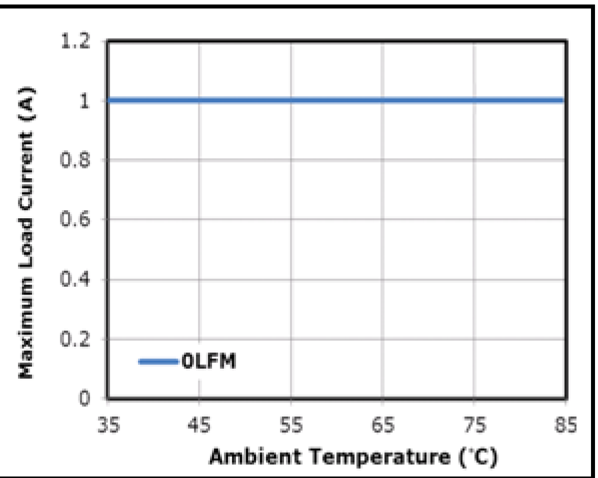

FIG.34 DE-RATING CURVE AT 12VIN

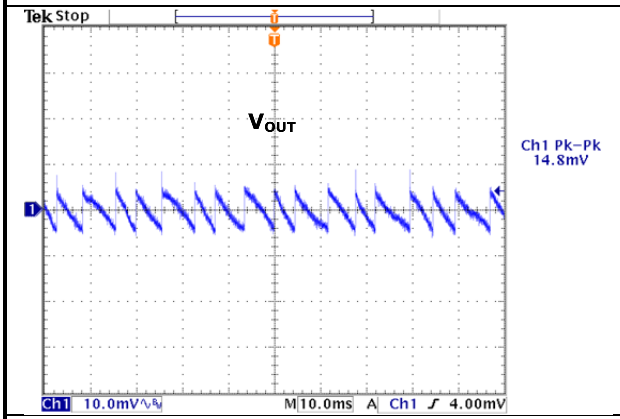

FIG.35 OUTPUT RIPPLE
(12VIN, IOUT=0A)

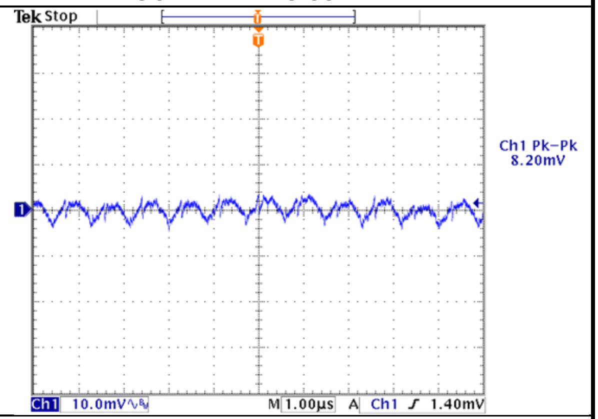

FIG.36 OUTPUT RIPPLE
(12VIN, IOUT=1A)

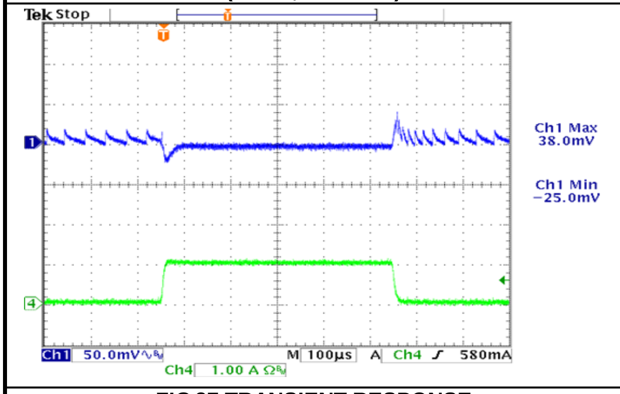

FIG.37 TRANSIENT RESPONSE
(12VIN, 0% to 100% LOAD STEP)

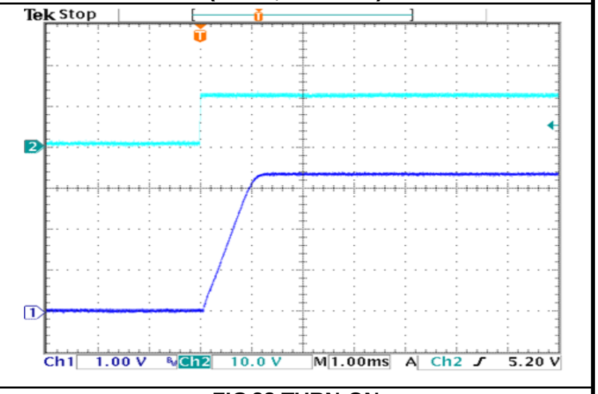

FIG.38 TURN-ON
(12VIN, IOUT=1A)

APPLICATIONS INFORMATION:

REFERENCE CIRCUIT FOR GENERAL APPLICATION:

Figure 39 shows the module application schematics for input voltage +12V and turn on by input voltage directly through enable resistor (REN).

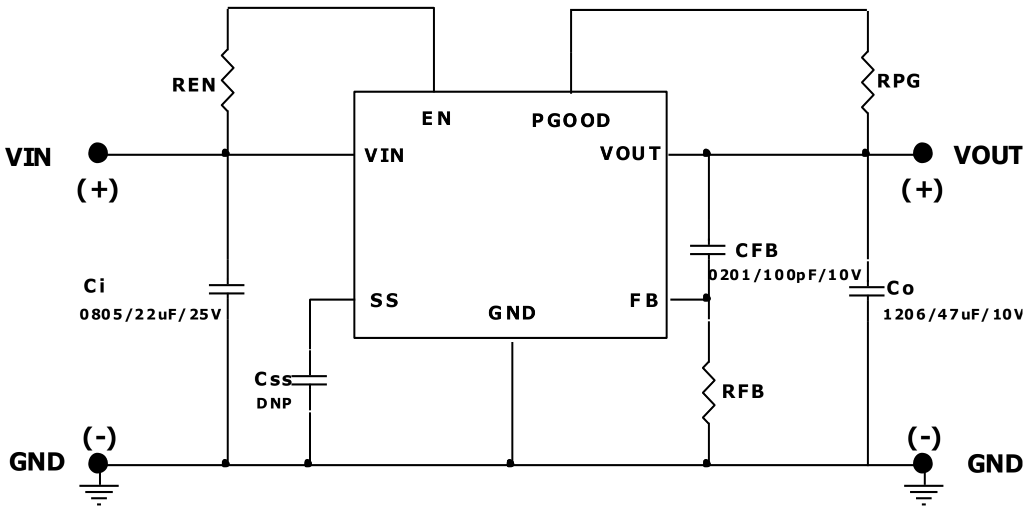

FIG.39 REFERENCE CIRCUIT FOR GENERAL APPLICATION

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1A, High Efficiency LDS Module

APPLICATIONS INFORMATION: (Cont.)

RECOMMENDATION LAYOUT GUIDE:

In order to achieve stable, low losses, less noise or spike, and good thermal performance some layout considerations are necessary. The recommendation layout is shown as Figure 40.

1. The ground connection between pin 5 and 9 should be a solid ground plane under the module. It can be connected one or more ground plane by using several Vias.
2. Place high frequency ceramic capacitors between pin 4 (VOUT), and pin 5, 9 (GND) for output side, as close to module as possible to minimize high frequency noise.
3. Keep the R_{FB} and C_{FB} connection trace to the module pin 2 (FB) short.
4. Use large copper area for power path (VIN, VOUT, and GND) to minimize the conduction loss and enhance heat transferring. Also, use multiple Vias to connect power planes in different layer.

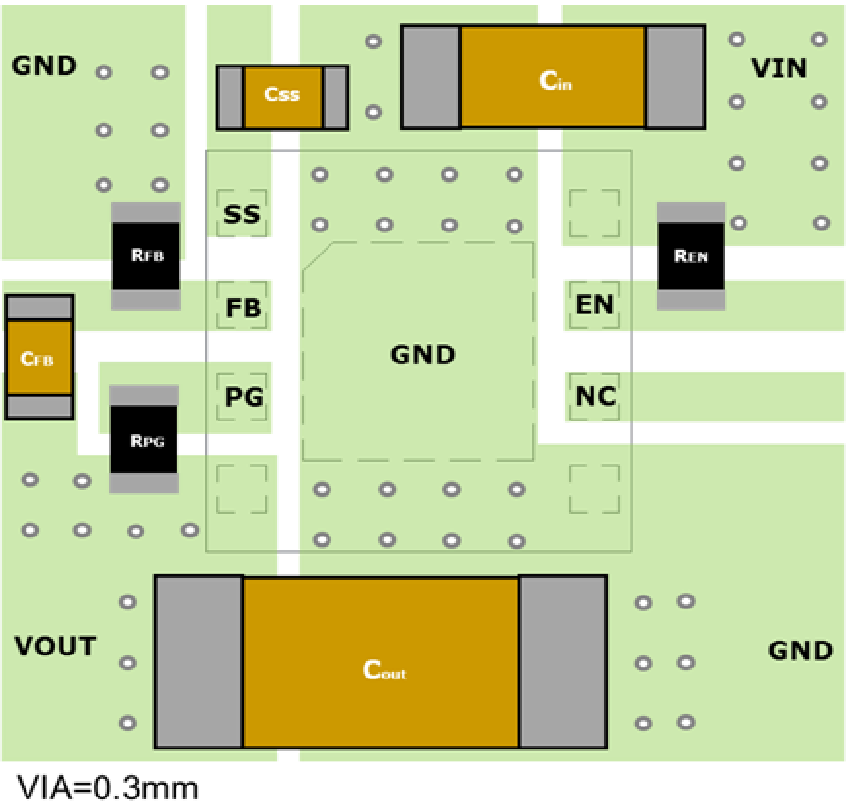

FIG.40 RECOMMENDATION LAYOUT

APPLICATIONS INFORMATION: (Cont.)

SAFETY CONSIDERATIONS:

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is the possibility of sustained input voltage reversal which is not current limited. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations.

For safety agency approvals, install the converter in compliance with the end-user safety standard.

INPUT FILTERING:

The module should be connected to a source supply of low AC impedance and high inductance in which line inductance can affect the module stability. An input capacitor must be placed as near as possible to the input pin of the module so to minimize input ripple voltage and ensure module stability.

OUTPUT FILTERING:

To reduce output ripple and improve the dynamic response as the step load changes, an additional capacitor at the output must be connected. Low ESR polymer and ceramic capacitors are recommended to improve the output ripple and dynamic response of the module.

PROGRAMMING OUTPUT VOLTAGE:

The module has an internal 0.6V±2% reference voltage. The output voltage can be programmed by the dividing resistor (RFB) which connects to both FB pin and GND pin. The output voltage can be calculated by Equation 1, resistor choice may be referred to TABLE 1.

$$\text{VOUT (V)} = 0.6 \times \left(1 + \frac{100\text{k}}{\text{RFB}}\right) \qquad \text{(EQ.1)}$$

VOUT (V)	RFB(kΩ)
1.0	150(1%)
1.2	100(1%)
1.8	50(1%)
2.5	31.6(1%)
3.3	22.1(1%)

TABLE 1 Resistor values for common output voltages

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APPLICATIONS INFORMATION: (Cont.)

Thermal Considerations:

All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 42mm×42mm×1.6mm with 4 layers. The case temperature of module sensing point is shown as Figure 41. Then $Rth(j_{choke}\text{-}a)$ is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The HU2103 power module is designed for using when the case temperature is below 110°C regardless the change of output current, input/output voltage or ambient temperature.

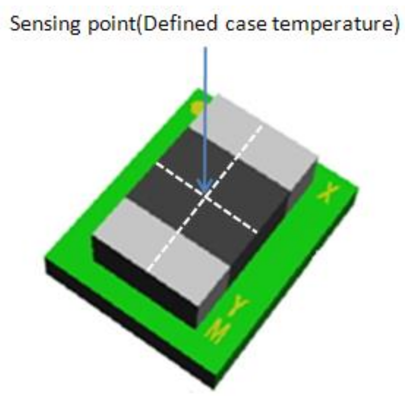

FIG. 41 Case Temperature Sensing Point

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REFLOW PARAMETERS:

Lead-free soldering process is a standard of making electronic products. Many solder alloys like Sn/Ag, Sn/Ag/Cu, Sn/Ag/Bi and so on are used extensively to replace traditional Sn/Pb alloy. Here the Sn/Ag/Cu alloy (SAC) are recommended for process. In the SAC alloy series, SAC305 is a very popular solder alloy which contains 3% Ag and 0.5% Cu. It is easy to get it. Figure 42 shows an example of reflow profile diagram. Typically, the profile has three stages. During the initial stage from 70°C to 90°C, the ramp rate of temperature should be not more than 1.5°C/sec. The soak zone then occurs from 100°C to 180°C and should last for 90 to 120 seconds. Finally the temperature rises to 230°C to 245°C and cover 220°C in 30 seconds to melt the solder. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and user could switch to optimize the profile according to various solder type and various manufactures' formula.

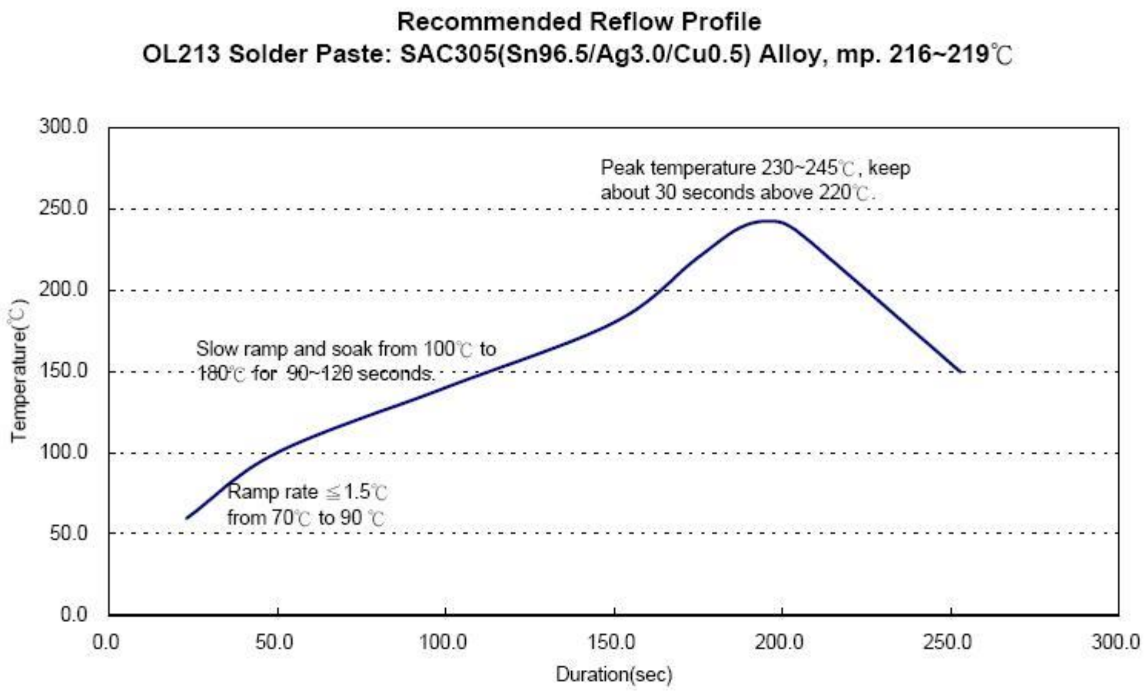

FIG.42 Recommendation Reflow Profile

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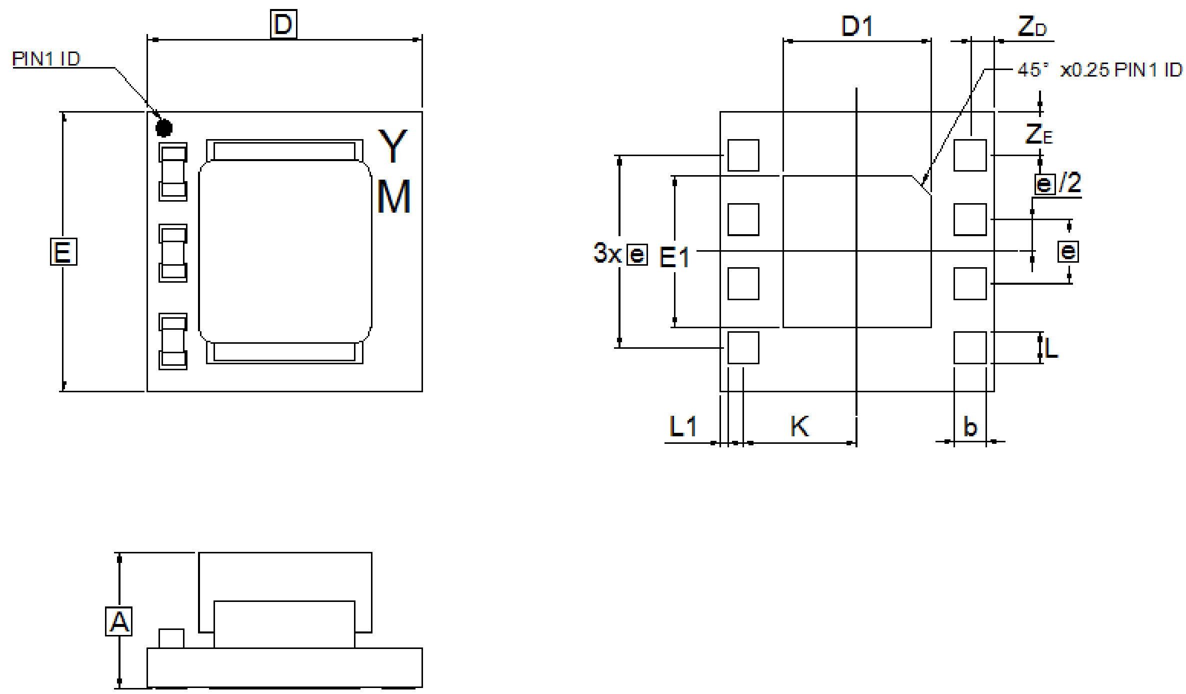
PACKAGE OUTLINE DRAWING:

Unit: mm



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.40	1.55	1.70
D	3.4	3.5	3.6
D1	1.80	1.9	2.00
E	3.4	3.5	3.6
E1	1.80	1.9	2.00
K	1.40	1.45	1.50
e	0.75	0.80	0.85
b	0.30	0.40	0.50
L	0.30	0.40	0.50
L1	0.05	0.10	0.15
ZD	0.20	0.30	0.40
ZE	0.45	0.55	0.65

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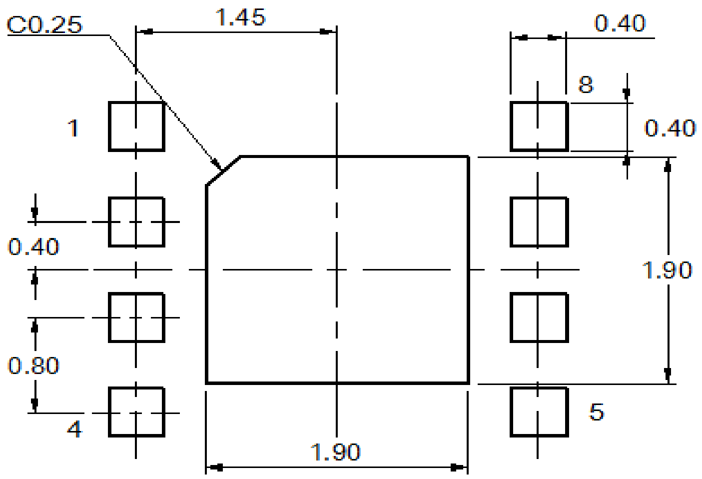
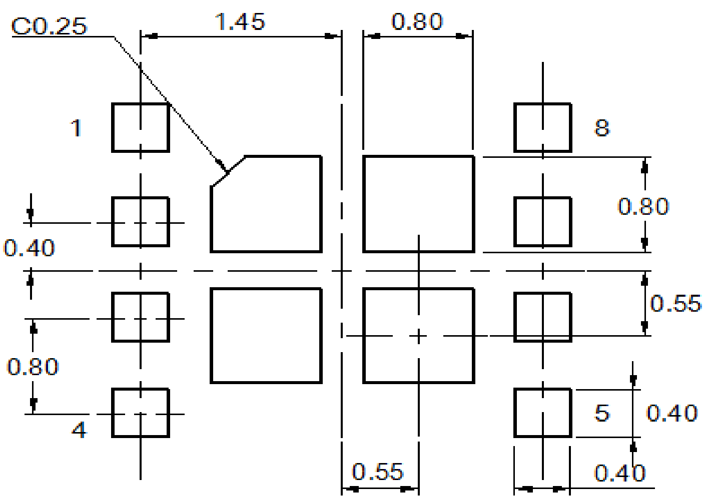
LAND PATTERN REFERENCE:

Unit: mm



RECOMMENDED LAND PATTERN



RECOMMENDED STENCIL PATTERN
BASED ON 130um THICK STENCIL

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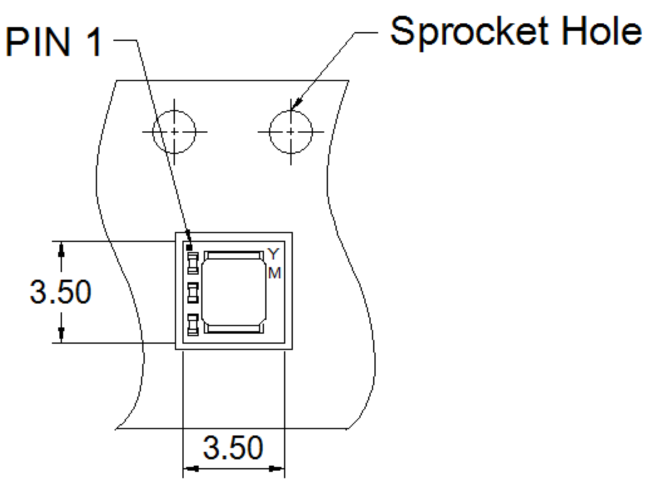
PACKING REFERENCE:

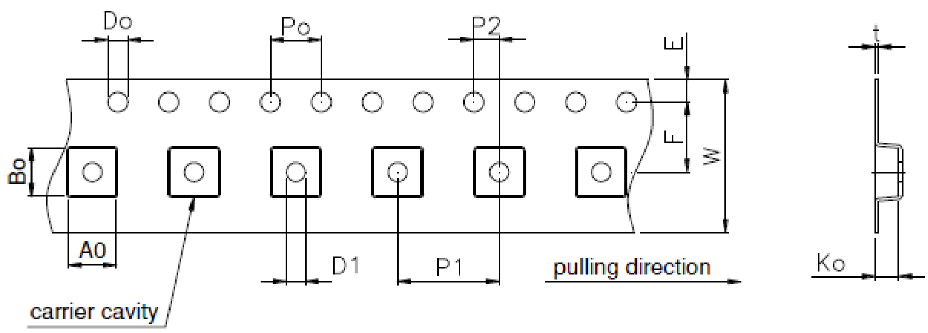
Unit: mm

Package In Tape Loading Orientation



Tape Dimension

Unit:mm



A0	3.8± 0.10	E	1.75 ± 0.10
B0	3.8 ± 0.10	K0	1.88 ± 0.10
F	5.50 ± 0.05	P0	4.00 ± 0.10
W	12.00 ±0.30	P1	8.00 ± 0.10
D0	φ1.55 ±0.05	P2	2.00 ± 0.05
D1	φ1.50± 0.10	t	0.25 ± 0.10

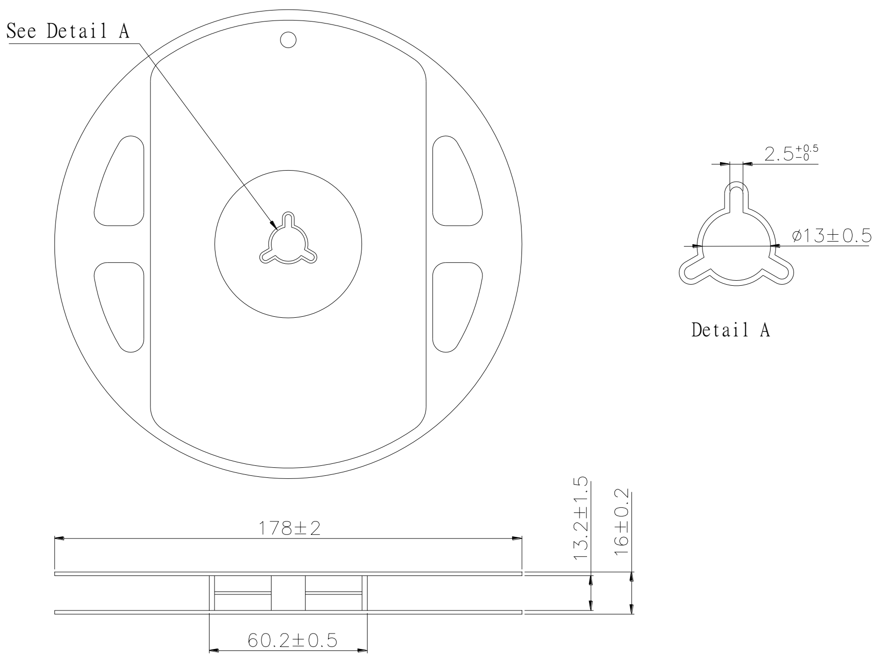
HU2103

1A, High Efficiency LDS Module

PACKING REFERENCE: (Cont.)

Unit: mm

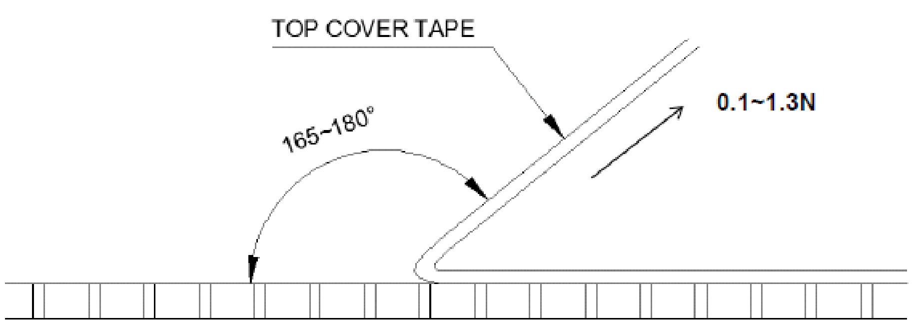
Reel Dimension



Peel Strength of Top Cover Tape

The peel speed shall be about 300mm/min.

The peel force of top cover tape shall be between 0.1N to 1.3N



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1A, High Efficiency LDS Module

REVERSION HISTORY:

Date	Revision	Changes
2014.06.24	00	Release the preliminary specification.
2014.07.09	01	Update application and POD drawing.
2014.09.17	02	Update Electrical specifications and packing information.
2014.11.24	03	Adjust Fig. sequence.
2014.12.11	04	Update land pattern reference.
2014.12.31	05	Update uPOL module to LDS module.
2015.02.26	06	Update POD and PIN 1 drawing.
2015.06.05	07	Update recommendation layout and schematic Change pin 6 define to N.C.
2015.06.24	08	Add REFLOW PARAMETERS